FIFO MEMORY DEVICES HAVING MULTI-PORT CACHE MEMORY ARRAYS THEREIN THAT SUPPORT HIDDEN EDC LATENCY AND BUS MATCHING AND METHODS OF OPERATING SAME

Abstract of the Disclosure

An integrated circuit memory device includes a quad-port cache memory device and a higher capacity supplemental memory device. These memory devices operate collectively as a high speed FIFO having fast fall through capability and extended data capacity. The FIFO does not require complex arbitration circuitry to oversee reading and writing operations. The supplemental memory device may be an embedded on-chip memory device or a separate off-chip memory device (e.g., DRAM, SRAM). The quad-port cache memory device utilizes a data rotation technique to support bus matching. Error detection and correction (EDC) circuits are also provided to check and correct FIFO read data. The EDC circuits operate without adding latency to FIFO read operations.

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